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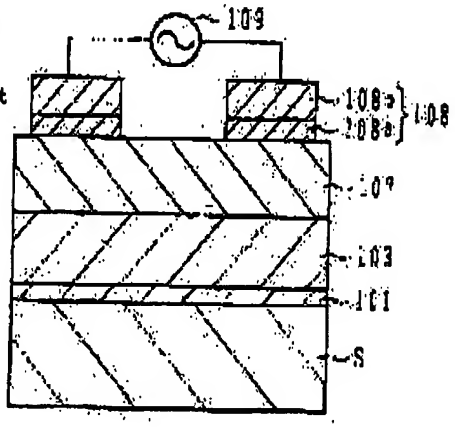
(54) SEMICONDUCTOR ELEMENT AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To form a semiconductor element having good ohmic electrode on a p type ZnO single crystal layer.
SOLUTION: The semiconductor element comprises a p type ZnO single crystal layer 107, a first metal layer 108a contacted with the layer 107 and containing at least one type selected from the group consisting of Ni, Rh, Pt, Pd and their alloys, and a second metal layer 108b formed on the layer 108a and containing a metal different from that of the layer 108a or their alloys.



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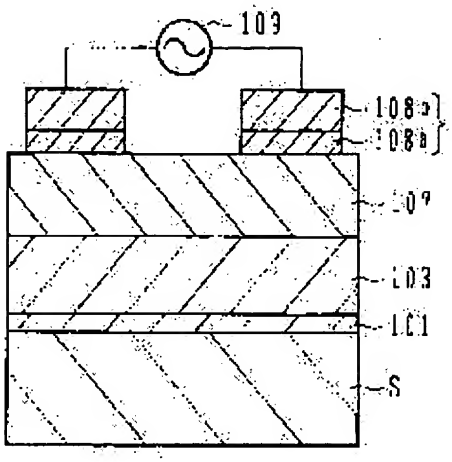

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CLAIMS

【Claim(s)】

【Claim 1】A semiconductor device comprising:

A p type ZnO system single crystal layer.

The 1st metal layer containing at least one sort which contacted said p type ZnO system single crystal layer, and was chosen from a group of nickel, Rh, Pt, Pd, and these

alloys.
Metal which is formed on said 1st metal layer and is different from said 1st metal layer, or the 2nd metal layer containing those alloys.

[Claim 2]A semiconductor device comprising:
A p type ZnO system single crystal layer.
The 1st metal layer in which said p type ZnO system single crystal layer is contacted, and a work function contains about 5.0-eV metal.
The 2nd metal layer that consists of an alloy containing one sort of different metal from metal which is formed on said 1st metal layer, and a work function is about 5.0 eV and forms said 1st metal layer, or these metal.
A surface metal layer which is formed on said 2nd metal layer and consists of metal in which the work function is lower than a work function of said 1st metal layer.

[Claim 3]The semiconductor device according to claim 2 which has the reflectance in which said surface metal layer is higher than said 2nd metal layer.
[Claim 4]The semiconductor device according to claim 2 containing an alloy containing an alloy in which said surface metal layer contains Ag or Ag, aluminum, or aluminum.
[Claim 5]A semiconductor device given in either to claims 2-4 containing a compound in which said work function contains elements in which about 5.0-eV metal is chosen from among nickel, Au, C, and Pd, or these elements, or

an alloy.

[Claim 6]A semiconductor device given in either to claims 1-5 stratified or whose heights of 50 nm or less of said 1st metal layer thickness is a field with an island shape of 50 nm or less.

[Claim 7]A semiconductor device given in either to claims 1-6 said whose 1st metal layer is nickel and in which said 2nd metal layer is Au.

[Claim 8]A semiconductor device given in either to claims 1-7 in which said 1st metal layer and said 2nd metal layer are in a **** state.

[Claim 9]A semiconductor device given in either to claims 1-8 by which said p type ZnO system single crystal is the laminated structure by which a ZnO layer and a ZnTe layer were laminated by turns, and N is doped by said ZnTe layer at least.

[Claim 10]A semiconductor device given in either to claims 1-8 by which ** doping of a p type impurity and the n type impurity is carried out as for said p type ZnO system single crystal.

[Claim 11]The semiconductor device according to claim 10 said whose p type impurity is N and in which said n type impurity is Ga.

[Claim 12]A manufacturing method of a semiconductor device including a process of forming the 2nd metal layer characterized by comprising the following.

A process for which a p type ZnO system single crystal layer to which the surface was exposed is prepared.

A process of forming the 1st metal layer containing at

least one sort chosen from a group of nickel, Rh, Pt, Pd, and these alloys on the surface of said p type ZnO system single crystal layer.
Different metal from said 1st metal layer on said 1st metal layer, or those alloys.

[Claim 13]A manufacturing method of a semiconductor device characterized by comprising the following.
A process for which a p type ZnO system single crystal layer to which the surface was exposed is prepared.
A process of forming the 1st metal layer in which a work function contains about 5.0-eV metal on the surface of said p type ZnO system single crystal layer.
A process of a work function being about 5.0 eV, and a work function being metal lower than a work function of said 1st metal layer, and forming the 2nd metal layer that consists of an alloy containing different metal from metal which forms said 1st metal layer, or these metal on said 1st metal layer.

[Claim 14]A manufacturing method of the semiconductor device according to claim 12 or 13 which includes a process of heat-treating, after a process of forming said 1st and 2nd metal layers.
[Claim 15]A semiconductor device comprising:
A substrate.
A ZnO system buffer layer formed on said substrate.
The 1st semiconductor layer containing the 1st conductivity type or a 2nd conductivity-type ZnO system

single crystal layer formed on said ZnO system buffer layer.

The 2nd semiconductor layer that is formed on said 1st conductivity type or a 2nd conductivity-type ZnO system single crystal layer, and has said 1st conductivity type or a conductivity type contrary to a 2nd conductivity-type ZnO system single crystal layer, The 1st metal layer containing at least one sort which contacted a p type semiconductor layer among said 1st semiconductor layer or said 2nd semiconductor layer, and was chosen from a group of nickel, Rh, Pt, Pd, and these alloys, Metal which is formed on said 1st metal layer and is different from said 1st metal layer, or the 2nd metal layer containing those alloys.

【Claim 16】It is formed on the 1st metal layer characterized by comprising the following, and said 1st metal layer, A semiconductor device containing the 2nd metal layer that consists of a kind of an alloy containing metal which a work function is about 5.0 eV and is different from metal which forms said 1st metal layer, or these metal, and a surface metal layer which it is formed on said 2nd metal layer, and a work function becomes from metal lower than a work function of said 1st metal layer.

A substrate.

A ZnO system buffer layer formed on said substrate.

The 1st semiconductor layer containing either of the 1st conductivity type or 2nd conductivity-type ZnO system single crystal layers which were formed on said ZnO system

buffer layer.

It is formed on said 1st conductivity type or a 2nd conductivity-type ZnO system single crystal layer, a p type semiconductor layer is contacted among said 1st semiconductor layer or said 2nd semiconductor layer including the 2nd semiconductor layer that has said 1st conductivity type or a conductivity type contrary to a 2nd conductivity-type ZnO system single crystal layer, and a work function is about 5.0-eV metal.

[Claim 17]the 2nd electrode characterized by comprising the following, and said 1st electrode -- and -- or an OPTO semiconductor device containing an opening formed in said 2nd electrode.

A substrate.

A ZnO system buffer layer formed on said substrate.

A n type ZnO system single crystal layer formed on said ZnO system buffer layer.

A p type ZnO system single crystal layer formed on said n type ZnO system single crystal layer, The 1st electrode in contact with said n type ZnO system single crystal layer, and the 1st metal layer containing at least one sort which contacted said p type ZnO system single crystal layer, and was chosen from a group of nickel, Rh, Pt, Pd, and these alloys, Metal which is formed on said 1st metal layer and is different from said 1st metal layer, or the 2nd metal layer containing those alloys.

[Claim 18]An OPTO semiconductor device comprising

containing the 2nd electrode and an opening formed in said 1st electrode and said 2nd electrode:

A substrate.

A ZnO system buffer layer formed on said substrate.

A n type ZnO system single crystal layer formed on said ZnO system buffer layer.

A p type ZnO system single crystal layer formed on said n type ZnO system single crystal layer, The 1st electrode in contact with said n type ZnO system single crystal layer, and the 1st metal layer in which said p type ZnO system single crystal layer is contacted, and a work function contains about 5.0-eV metal, The 2nd metal layer that consists of an alloy containing different metal from metal which is formed on said 1st metal layer, and a work function is about 5.0 eV and forms said 1st metal layer, or these metal, A surface metal layer which is formed on said 2nd metal layer and consists of metal in which a work function is lower than a work function of said 1st metal layer.

【Claim 19】The OPTO semiconductor device according to claim 17 or 18 with which said substrate is a transparent substrate and a reflector which reflects in said substrate side light emitted from said opening on said opening is provided.

【Claim 20】While a reflection part which reflects in the rear-face side of said substrate light which he follows towards said substrate is provided, to the surface side of said substrate. The OPTO semiconductor device

according to claim 17 or 18 with which the 2nd transparent substrate in which the 1st wiring section that contacts said 1st electrode and said 2nd electrode electrically, respectively, and the 2nd wiring section were formed is arranged.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to a semiconductor device which includes in details the electrode structure from which low resistance ohmic contact is obtained to a p form ZnO system single crystal more, and a manufacturing method for the same about the semiconductor device of a ZnO system.

[0002]

[Description of the Prior Art]As for the ZnO crystal which is a kind of II-VI group compound semiconductor, the application to OPTO semiconductor devices, such as a light emitting device and a photo detector, is expected. Since a ZnO crystal is a semiconductor which has a large band gap (Eg = 3.4 eV), the luminous wavelength corresponding to a band gap serves as 360 to 400-nm ultraviolet radiation.

[0003]

[Problem(s) to be Solved by the Invention]By the way, ZnO has the character called unipolarity. Although it was comparatively easy to realize an n-type semiconductor (n-ZnO) using ZnO, it was difficult to realize a p-type

semiconductor (p-ZnO).

[0004]Therefore, it was difficult to form p-n junction using ZnO, and it difficult to realize the semiconductor device of a ZnO system, especially the OPTO semiconductor device which has p-n junction.

[0005]The report of that the p type ZnO crystal was obtained is made by using into ZnO the art which carries out the ** dope (co-dope) of the gallium (Ga) which is nitrogen (N) and the n type impurity which are p type impurities these days. The method of more specifically growing up a p type ZnO single crystal by the pulse laser deposition method, carrying out the ** dope (co-dope) of the gallium (Ga) which is nitrogen (N) and the n type impurity which are p type impurities into ZnO is used.

[0006]By the way, although aluminum was generally used as an ohmic electrode to a n type ZnO crystal, there was no knowledge about the ohmic electrode which fitted the p type ZnO crystal from the above situations.

[0007]An object of this invention is to provide a semiconductor device which has ohmic electrode structure suitable for a p type ZnO system crystal, and a manufacturing method for the same.

[0008]

[Means for Solving the Problem]The 1st metal layer containing at least one sort which contacted a p type ZnO system single crystal layer and said p type ZnO system single crystal layer according to one viewpoint of this invention, and was chosen from a group of nickel, Rh, Pt, Pd, and these alloys, It is formed on said 1st metal layer,

and a semiconductor device containing different metal from said 1st metal layer or the 2nd metal layer containing those alloys is provided.

[0009]A process for which a p type ZnO system single crystal layer to which the surface was exposed is prepared according to other viewpoints of this invention, A process of forming the 1st metal layer containing at least one sort chosen from a group of nickel, Rh, Pt, Pd, and these alloys on the surface of said p type ZnO system single crystal layer, A manufacturing method of a semiconductor device including different metal from said 1st metal layer on said 1st metal layer or the 2nd metal layer containing those alloys, and a process to form is provided.

[0010]A ZnO system buffer layer which was formed on a substrate and said substrate according to other viewpoints of this invention, The 1st semiconductor layer containing either of the 1st conductivity type or 2nd conductivity-type ZnO system single crystal layers which were formed on said ZnO system buffer layer, It is formed on said 1st conductivity type or a 2nd conductivity-type ZnO system single crystal layer, and the 2nd semiconductor layer that has said 1st conductivity type or a conductivity type contrary to a 2nd conductivity-type ZnO system single crystal layer is included, The 1st metal layer containing at least one sort which contacted a p type semiconductor layer among said 1st semiconductor layer or said 2nd semiconductor layer, and was chosen from a group of nickel, Rh, Pt, Pd, and these alloys, It is formed on said 1st metal layer, and a semiconductor device

containing different metal from said 1st metal layer or the 2nd metal layer containing those alloys is provided.

[0011]

[Embodiment of the Invention]Hereafter, the term with the p type ZnO system single crystal used in this specification shall also contain not only a p type ZnO single crystal but the semiconductor single crystal layer which has the same large band gap as ZnO, for example like the superstructure of ZnO and ZnTe including ZnO as a basic component.

[0012]"The growing temperature of the low-temperature growth ZnO" defined in this specification is a temperature lower about 400 ** than temperature with a crystal growth [for generally growing up a ZnO single crystal] of 200 to about 600 ** from 100 **, for example. "Growing temperature of a high temperature growth single crystal ZnO layer" is the growing temperature for which it was suitable when growing up a ZnO single crystal generally, and is a temperature lower than 800 ** higher than the above-mentioned "growing temperature of the low-temperature growth ZnO" and, for example, is 650 **.

[0013]The artificer performed examination about the electrode for p type ZnO semiconducting crystals first.

[0014]When joining metal (electrode) and a semiconductor, the barrier height eVd seen from the semiconductor side is expressed with eVd=phi m-phi s. Here, as for the diffusion potential of a semiconductor layer, and phim, a metaled (electrode) work function and phis of Vd are the work functions of a semiconductor.

[0015] When a p-type semiconductor and metal are contacted, the conditions from which good ohmic junction is acquired are expressed with phim>phis (p).

[0016] By the way, work function phi of a p type ZnO semiconducting crystal is (p) is as large as about 6.25 eV (when an intrinsic semiconductor is assumed). If the doped quantity of a p type impurity is assumed to be $10^{18}cm^{-3}$, it will become about phis7.9 eV of work functions. Therefore, as an ohmic electrode material for p type ZnO system single crystals, it is considered to be desirable also from a viewpoint of reducing the contact resistance between metal-semiconductors to choose the comparatively large metal of a work function (phim).

[0017] As an ohmic electrode material for p type ZnO system single crystals, specifically, nickel (phim=5.15), germanium (phim=5.0), Se (phim=5.9), Since materials, such as Rh (phim=4.98), Te (phim=4.95), Re (phim=4.96), Ir (phim=5.27), Pt (phim=5.65), Au (phim=5.1), C (phim=5.0), and Pd (phim=5.12), have the comparatively large work function, it is thought that it is desirable.

[0018] Work functions are within the limits from 4.5 to 6.0, and the description as used herein "a work function is about 5.0 eV" means preferably that work functions are within the limits from 4.9 to 5.2, for example.

[0019] According to the theoretical consideration and the experimental result by an artificer, especially the laminated structure of nickel (1st layer: metal which carries out direct contact to p type ZnO crystal)/Au (two-layer eye: metal deposited on the metal of the 1st

layer) is preferred.

[0020]It turned out that what heat-treated to the laminated structure of Rh/Au, Pt/Rh, Pd/Au, Pt/Au, nickel/Rh, nickel/Pt, nickel/Pd, nickel/Ir, Ir/Au, Ir/Rh, and Ir/Pd other than the structure which heat-treated to the laminated structure of Ti/Au is promising.

[0021]Based on the above knowledge, the semiconductor device which has the above electrode structures as an ohmic electrode to a p type ZnO system single crystal is explained below.

[0022]The semiconductor device by a 1st embodiment of this invention is explained with reference to drawings.

[0023]as an example of the growth device for growing up the ZnO system crystal structure which constitutes a semiconductor device to be drawing 1 -- radical sauce molecular beam epitaxy (RS-MBE) -- the structure of the crystal growth device (henceforth "a RS-MBE device") using law is shown.

[0024]The RS-MBE device A is provided with the following.
The chamber 1 to which crystal growth is performed.
Vacuum pump P which maintains the chamber 1 at an ultrahigh-vacuum state.

[0025]The chamber 1 is provided with the following.
The port 11 for Zn for evaporating Zn.
The port 21 for Ga for evaporating Ga.
The O radical port 31 for irradiating with O radical.
The N radical port 41 for irradiating with N radical.

[0026]The port 11 for Zn is provided with heating, and Knudsen cell (Knudsen cell: call it K cell below.) 17 and shutter S_1 to evaporate while it accommodates the Zn (purity 7N) raw material 15.

[0027]The port 21 for Ga the O radical port 31 provided with the K cell 27 heated and evaporated while accommodating Ga raw material 25, and shutter S_2, The oxygen gas which is material gas is introduced in an electrodeless discharge lamp, and O radical generated using high frequency (13.56 MHz) is spouted in the MBE chamber 1. The orifice 33 and shutter S_3 are provided to the beam of O radical.

[0028]The N radical port 41 introduces the nitrogen gas which is material gas in an electrodeless discharge lamp, and spouts N radical generated using high frequency (13.56 MHz) in the MBE chamber 1. Shutter S_4 is provided to the beam of N radical.

[0029]The structure of the radical ports 31 and 41 is the structure where the induction coil is wound around the outside of the discharge tube provided in the outside sealed tube.

[0030]In the chamber 1, the substrate holder 3 holding sapphire substrate S used as the ground of crystal growth and the heater 3a for heating the substrate holder 3 are formed.

[0031]It is indirectly measurable in the temperature of sapphire substrate S by the thermo couple 5 installed in the heater. The position of the substrate holder 3 is movable by the manipulator 7 which used bellows.

[0032]The chamber 1 contains the cancer 51 of a reflection-electron-diffraction device (RHEED device) established in order to monitor the grown-up crystal layer, and the screen 55 of a RHEED device. It can grow up using the cancer 51 of a RHEED device, and the screen 55 of a RHEED device, monitoring the situation (an amount of growth, the quality of the grown-up crystal layer) of the crystal growth within the MBE device A.

[0033]The temperature of crystal growth, the thickness of a crystal growth film, the degree of vacuum in a chamber, etc. are suitably controlled by the control device C.

[0034]Below, the process of growing up ZnO on sapphire substrate S is explained in detail.

[0035]Crystal growth is performed by opening and closing from shutter S_1 to S_4 suitably by RS-MBE technique.

[0036]RF-MBE technique using RF as a method of generating radical sauce is used. O radical is generated by introducing O_2 which is material gas in an electrodeless discharge lamp using 13.56-MHz high frequency. By making O radical blow off in the MBE chamber 1 of a high vacuum state, it becomes O radical beam. A ZnO thin film is grown up by irradiating with O radical beam and Zn beam from K cell simultaneously on sapphire substrate S.

[0037]Drawing 2 is a sectional view showing the structure of the semiconductor device by this embodiment.

[0038]The process for forming in below the semiconductor device shown in drawing 2 is explained.

[0039]1) Surface treatment: (0001) Wet etching of the sapphire substrate S surface which has a field was carried

out for 60 minutes in the solution of H_3PO_4:H_2SO_4=1:3 heated at 110 **.

[0040]After performing the above-mentioned surface treatment, the substrate holder 3 (drawing 1) was equipped with sapphire substrate S.

[0041]The substrate temperature of 600 ** and the flow of oxygen were set to 2sccm, RF power was set in the MBE device under the conditions of 150W, and the surface treatment by oxygen plasma was performed for 1 hour. The sapphire substrate S surface is defecated by processing the surface of sapphire substrate S in an MBE device.

[0042]2) Low-temperature growth ZnO buffer layer growth: The buffer layer 101 is first grown up after the above-mentioned substrate surface treatment. Unlike the growing condition of the usual single crystal ZnO board, growth under low temperature and Zn Rich's conditions is performed (low-temperature growth ZnO layer). The beam amount of Zn is 4.0×10^{-7}Torr.

[0043]RF plasma source of O is used as a supply source of an oxygen beam. Pure oxygen (purity 6N) gas is introduced into the O radical port 21, and it becomes radical using a high frequency oscillation source.

[0044]In flow 2.0sccm, 5×10^{-5}Torr and the RF power of the flow of oxygen which is gas sauce are 300W as a partial pressure of oxygen in a chamber. Growing temperature was performed at 500 **. It is preferred to perform growth among 200 to 600 **.

[0045]The thickness of the ZnO buffer layer 101 was 10 nm. The range of thickness of 10 to 100 nm is preferred.

[0046]Here, the value of the above-mentioned pressure shows the indicated value of the nude ion gage attached to the substrate holder position (growth position).

[0047]3) Flattening processing: After growing up the low-temperature growth ZnO buffer layer 101, flattening processing of the surface of the ZnO buffer layer 101 was performed. Heat treatment for 10 minutes was performed in an elevated temperature into which a single crystal is grown up as flattening processing, for example, 600 **. Heat treating time is chosen from the time for 60 minutes after for 2 minutes.

[0048]The low-temperature growth ZnO buffer layer 101 which finished growth with low growing temperature is a single crystal which has a grain boundary, and is considered to grow epitaxially so that the anisotropy with each same grain may be shown. It mainly originates in the grain boundary between the grain, and unevenness is observed. It is thought that the single crystal of each grain carries out solid phase growth, a grain size is enlarged, and flattening of the surface is carried out by performing the above-mentioned heat treatment to the low-temperature growth ZnO buffer layer 101.

[0049]Since the original surface unevenness is small compared with the case where it is made to grow up on condition of oxygen Rich when it is made to grow up especially on condition of Zn Rich, the flat surface outstanding by flattening processing is easy to be obtained. If a ZnO layer is grown up at an elevated temperature on the low-temperature growth ZnO buffer

layer which has the outstanding planar surface, a good crystalline single crystal ZnO layer will be easy to be obtained.

[0050]In the state where it has grown up (as-grown), since a grain size is small and a grain boundary is observed, the low-temperature growth ZnO buffer layer 101 looks also like polycrystal by observation (AtomicForceMicroscopy:AFM). However, when analysis by the X diffraction or the RHEED method is conducted, the characteristic of a single crystal is shown.

[0051]This phenomenon is observed in growth by GaN or ZnO. By carrying out high temperature heat treatment of the low-temperature growth ZnO buffer layer 101, it grows up like the case where unevenness resulting from a grain boundary etc. is solid phase growth, and it is thought that the surface carries out flattening. Even if it is going to grow up the single crystal ZnO on the ZnO surface which is not flat, the crystallinity does not become good on experience.

[0052]4) Growth of a undoped ZnO single crystal layer: It ranked second and the single crystal (high-temperature-growth ZnO single crystal layer) 103 of undoped ZnO was grown up on the low-temperature growth ZnO buffer layer 101 which carried out flattening. Thickness is 1 micrometer.

[0053]As a growing condition, substrate temperature is 600 **. The temperature of K cell is 320 **. The vapor rate of Zn in this case is 1.6 A/second.

[0054]The flow of oxygen is 2.0sccm. In this case, the

partial pressure of oxygen is 5×10^{-5}Torr. RF power is 300W.

[0055] As a growing condition of the high-temperature-growth ZnO single crystal layer 103, it is the temperature between 600 to 800 **, and about 1 micrometer grows.

[0056] After forming the low-temperature growth ZnO buffer layer 101 and performing flattening processing of the surface, the crystallinity of the undoped ZnO single crystal layer 103 improved by growing up the ZnO single crystal layer 103 of high-temperature-growth undoping with high growing temperature on it.

[0057] When many crystal defects are introduced during a ZnO crystal, n type strong conductivity is shown also in the state where an impurity is not introduced. The high-temperature-growth undoped ZnO single crystal layer 103 grown-up using the above-mentioned crystal growth method has dramatically few crystal defects. In the ZnO single crystal grown-up with the conventional crystal growth method, it also becomes possible to realize ZnO which shows the p type difficult conductivity. Since a crystal defect which forms a nonluminescent center is reduced substantially, it is thought that luminous efficiency also became very high.

[0058] 5) Growth of a p type ZnO single crystal layer: Next, the p type ZnO single crystal layer 107 was grown up.

[0059] The growing condition of the p type ZnO single crystal layer 107 is the same as the growing condition of the above-mentioned undoped ZnO single crystal layer 103 almost.

[0060] However, crystal growth was performed at 550 **. As growing temperature, the range of 500 to 700 ** is preferred.

[0061] In addition to Ga which is usually a dopant for n type ZnO, N was used as a dopant. K cell temperature of Ga is 600 **. In ZnO crystal growth, N plasma was introduced in the chamber and N was doped. The flows of N_2 gas at the time of generating N plasma are 0.1sccm and RF power 300W. Thickness is 1 micrometer.

[0062] Evaluation by hole measurement was performed about the grown-up p type ZnO single crystal 107. It was checked that p type conductivity is actually shown. Resistivity is 1.78-ohmcm. P type impurity concentration is $5.47 \times 10^{17} cm^{-3}$.

[0063] By optimizing crystal growth conditions, it is expected that the p type ZnO single crystal layer of the impurity concentration of higher impurity concentration, for example, a $10^{19} cm^{-3}$ grade, is obtained.

[0064] 6) Formation of an ohmic electrode : rank second and explain the process of forming an electrode on the p type ZnO single crystal layer 107.

[0065] First, after growing up to the pZnO single crystal layer 107, sapphire substrate S is taken out from the MBE chamber 1 (drawing 1). After forming the mask pattern for vacuum evaporation, sapphire substrate S is attached in an evaporation apparatus.

[0066] In an evaporation apparatus, nickel is vapor-deposited by a thickness of 70 A as the 1st metal layer 108a on a p type ZnO single crystal. Subsequently,

3500A of Au(s) are formed as the 2nd metal layer 108b. Two or more nickel / Au electrodes 108 are formed in the position which left only prescribed distance.

[0067]The substrate with which nickel / Au electrode 108 was formed was taken out from the inside of an evaporation apparatus, and the substrate was heat-treated with lamp heating in a nitrogen atmosphere. Cooking temperature is 500 ** and cooking time is 20 seconds.

[0068]It is also possible to use an independent material, for example, Au, as the above-mentioned electrode material.

[0069]When heat-treating, heating conditions can be performed in 200 to 600 **. The range of 300 to 500 ** is preferred. It is desirable to perform heat treatment under the atmosphere of inactive gas, such as nitrogen (N_2) and argon (Ar).

[0070]Since ZnO is used as the crystalline material, it is also possible to heat-treat under [, such as inside of the atmosphere and the bottom of oxygen gas atmosphere,] existence of oxygen gas. If it heat-treats under existence of oxygen gas, dissociation of oxygen from a ZnO crystal can be prevented.

[0071]The cooking time in the case of heat-treating is from 1 second before 10 minutes. It is preferred for 1 second to 3 minutes that it is less than 1 minute preferably practical.

[0072]The result of having evaluated the electrical property of nickel / Au electrode 108 formed on the p type ZnO crystal layer 107 formed in drawing 3 of the

above-mentioned process using the measuring instrument 109 (drawing 2) is shown.

[0073]The sizes of a sapphire substrate are 10 mm x about 12 mm. On this sapphire substrate, two or more nickel / Au electrodes 108 (drawing 2) which aligned in the lengthwise direction and the transverse direction in a 5-mm pitch were formed.

[0074]The size of each electrode is phi0.1mm. Inter-electrode current/voltage characteristics were evaluated among these electrodes using the electrode of a couple. Drawing 3 shows the current/voltage characteristics acquired at this time. The ohmic characteristic almost linear as a result was obtained.

[0075]The value of the contact resistance surveyed at this time is an abbreviation 3.3komega grade. The called-for contact resistivity is abbreviation $1x10^{-2}$omegacm^2.

[0076]As mentioned above, if p type impurity concentration is made high by optimizing the growing condition of the p type ZnO single crystal layer 107, the sheet resistance of the p type ZnO single crystal layer 107 will become still lower. In addition, the contact resistance between the p type ZnO single crystal layer 107, and the nickel/Au electrode 108 is reduced further.

[0077]In the semiconductor device by a 1st embodiment of above-mentioned this invention, although the two-layer laminated structure of nickel/Au was used as an ohmic electrode for p type ZnO single crystals, By heat treatment after electrode formation, the electrode structure of nickel/Au may form the alloy film of **** one,

and the laminated structure may be maintained. With the alloy film which harmonized completely, it may react to a p type ZnO system single crystal or the controlled atmosphere at the time of heat treatment, and the alloy film which contains a part of these in a component may be included. For example, a laminated structure is contained by a certain factor (for example, thermal energy added at the time of heat treatment), homogeneous diffusion or also when it carries out counter diffusion and the order nature as a laminated structure is lost.

[0078] As mentioned above as an ohmic electrode material on a p type ZnO single crystal, Rh/Au, Pt/Rh, Pd/Au, Pt/Au, nickel/Rh, nickel/Pt, nickel/Pd, nickel/Ir, Ir/Au, Ir/Rh, the thing that heat-treated to the laminated structure of Ir/Pd, etc. can be used.

[0079] The metallic material listed into the electrode material of the 1st above-mentioned field at the next can also be doped. For example, B which is an III fellows compound and V fellows compound, aluminum, Ga, In, Y, P, As, Sb, Bi, V, Nb, Ta, etc. are mentioned.

[0080] The structure using the above electrodes shall also go into the range of this invention.

[0081] Ag and aluminum can also be used as a metallic material with high reflectance.

[0082] As for the ohmic electrode for p type ZnO system single crystals, electrodes, such as nickel/Au, should just touch on a p type ZnO system single crystal layer, for example.

[0083] The gestalt of an ohmic electrode may have which

gestalten, such as stratified, island shape, and an alloy, for example. In particular, after heat treatment, the ohmic electrode is island shape and a gestalt like an alloy in many cases. Actually, it becomes difficult to define the thickness of each electrode material itself correctly.

[0084] When mass production nature etc. are taken into consideration, it is a case where the most suitable process condition vapor-deposited about 200A of nickel within the limits of the experiment which the artificer conducted, vapor-deposited about 3000A of Au(s) after that, and it heat-treats after that.

[0085] The heat treatment front stirrup can also use the structure which forms metallic materials, such as Au, via metallic materials, such as Ti or W, as a metallic material for bonding pads after heat treatment if needed.

[0086] When the above-mentioned metallic material (Ti/Au or W/Au) is deposited before heat treatment, it is also considered that the metallic material and ohmic electrode material for bonding pads are spread mutually, and form a still more complicated alloy by heat treatment performed after that.

[0087] In this specification, the material (for example, nickel in the above-mentioned embodiment) which touches a p type ZnO system single crystal is called the 1st metal layer, and the metallic material formed on it is called the 2nd metal layer.

[0088] The metallic material which constitutes it is carrying out direct contact of the 1st metal layer to the p type ZnO system single crystal layer. Therefore, when

forming an ohmic electrode, the 1st metal layer plays the role most important for the ohmic characteristic etc.

[0089]However, the metallic material of the 1st layer is not actually restricted to what has a stratified gestalt as mentioned above. For example, when vapor-depositing the metallic material of the 1st layer in a vacuum evaporation in a plane, and the thickness planned is thin, a metallic material does not necessarily accumulate in layers over the whole surface on the surface of ZnO. Rather, a metallic material is formed in the shape of an island in many cases.

[0090]A thin thing is important for the thickness of the metallic material of a first pass eye, and it contacted the big metallic material of a work function, and the p type-ZnO layer of high hole carrier density, and is presumed to be that in which ohmic contact is formed by the work like a tunnel.

[0091]In using a thin metallic material as the 1st metal layer, the 2nd metal layer that had a certain amount of thickness on the 1st metal layer practically is needed. The influence which it has on the ohmic characteristic does not have a large metallic material which forms the 2nd metal layer compared with the metallic material which forms the 1st metal layer. However, it is preferred to use an above-mentioned metallic material in practice.

[0092]The method of depositing the alloys (nickel-Au alloy etc.) of the metallic material which forms the 1st above-mentioned metal layer on a p type ZnO single crystal, and the metallic material which forms the 2nd

above-mentioned metal layer, for example by sputtering process is also effective.

[0093]In the above-mentioned example, the p type ZnO system single crystal was formed by the method of Ga and N which carries out a ** dope while growing up the ZnO system single crystal.

[0094]In addition, the p type ZnO system single crystal which has the characteristic almost equivalent to a p type ZnO single crystal can be formed using the method explained below.

[0095]The crystal growth device used for growth of a p type ZnO system single crystal is the same device as an above RS-MBE device (drawing 1). However, Te is put instead of Ga in the port 21 for Ga in drawing 1. The purity of Te is 6N. A RS-MBE device is provided with the K cell 27 and shutter S_2 which carry out heating evaporation of the Te while it accommodates raw material Te (25). It can grow up using the RHEED cancer 51 and the RHEED screen 55 which were attached in the MBE device, monitoring the situation (an amount of growth, the quality of the grown-up crystal layer) of the crystal growth within the MBE device A.

[0096]The temperature of crystal growth, the thickness of a crystal growth film, the degree of vacuum in a chamber, etc. are suitably controlled by the control device C.

[0097]Below, the process of growing up a p type ZnO system single crystal layer on a ZnO board is explained.

[0098]All crystal growth is performed by an MBE technique.

[0099]The beam amount of Zn is 1.0×10^{-7}Torr, and the beam amount of Te is 5.0×10^{-7}Torr.

[0100]RF plasma source of O is used as a supply source of an oxygen beam. Pure oxygen (purity 6N) gas is introduced into the O radical port 31, and it becomes radical using a high frequency oscillation source.

[0101]RF plasma source of N is used as a supply source of a nitrogen beam. Pure nitrogen (purity 6N) gas is introduced into the N radical port 41, and it becomes radical using a high frequency oscillation source.

[0102]Oxygen (flow 2sccm) is [5x10 $^{-5}$Torr and nitrogen (flow 0.03sccm) of the pressure in the port 31 and 41 of oxygen which is gas sauce, and nitrogen] 2x10 $^{-6}$Torr(s) respectively. Growing temperature is 600 **.

[0103]Here, the value of the above-mentioned pressure shows the indicated value of the nude ion gage attached to the substrate holder position (growth position).

[0104]Although the unit of sccm was used as a flow of the above-mentioned gas sauce, this shows the flow in 25 ** and 1 atmosphere as everyone knows.

[0105]Drawing 4 shows two kinds of growing processes ((a) and (b)) for growing up a ZnO crystal by the opening-and-closing sequence of shutter S_1 to S_4.

[0106]Drawing 4 (a) shows the 1st growing process of two kinds of growing processes. To time t_1, shutter S_1 of Zn and shutter S_3 of O are opened. Elemental Zn and O element come flying on the substrate 100 surface, and a ZnO crystal layer grows. A ZnO crystal grows per molecular layer by controlling growing parameters, such as Zn amount of supply and O amount of supply.

[0107]One molecular layer means the crystal unit which

comprises one atomic layer of Zn, and one atomic layer of O on these specifications. Shutter S_1 and S_3 are opened until the crystal of ten molecular layers grows.

[0108] Shutter S_3 of O is closed in time t_2, and only Zn is supplied before time t_3. The end face of Zn is formed in the undoped ZnO layer 101a outermost surface as a result of Zn supply. Since it is desorbed from superfluous Zn, all the shutters are closed from t_3 before t_4. In time t_4, shutter S_2 of Te and shutter S_4 of N are made open, and Te and N are supplied on the end face of Zn. When Zn end face, Te, and N join together, one molecular layer of ZnTe layers by which N was doped grow.

[0109] in addition -- the RHEED pattern of a ZnTe layer is (2x1) in time t_4 -- Te -- a rich state is shown.

[0110] All the shutters are closed from t_5 before t_6, it ****s and an excessive atom is exhausted. Then, shutter S_1 of Zn is opened again and the end face of ZnTe is corrected. The surface which is Te Rich is changed into Zn Rich's surface. This makes surface morphology and a polar improvement.

[0111] Next, shutter S_3 of O is made open (t_7) and ZnO is grown up again. This state is equivalent to the state of time t_1. The above process is repeated 30 times.

[0112] By passing through the above process, a p type ZnO system single crystal can be grown up.

[0113] The second growing process is shown in drawing 4 (b). The outline of a growing process is shown below.

[0114] Shutter S_1 of Zn is opened and it changes into the state where elemental Zn were continuously supplied on the

substrate. Shutter S_3 of O is opened by time t_2, O element is supplied and ZnO by which impurity doping is not carried out positively is grown up.

[0115] Subsequently, after closing shutter S_3 of O by time t_2 and suspending supply of O element, shutter S_2 of Te and shutter S_4 of N are opened by time t_4, and the ZnTe layer which supplies Te element and N element and by which N was doped is grown up.

[0116] Shutter S_3 and S_4 are closed from time t_5 before t_6, and the end face of ZnTe is corrected.

[0117] Next, shutter S_3 of O is made open (t_7) and ZnO is grown up again. This state is equivalent to the state of time t_1. The above process is repeated 30 times.

[0118] In forming the ZnO buffer layer 101, after supplying Zn and O on the substrate 100 beforehand and growing up the ZnO layer of desired thickness, the above-mentioned process is performed.

[0119] As for the p type ZnO system single crystal layer formed after passing through either of the above two processes, ZnTe is laminated for ZnO at a rate of one molecular layer to ten molecular layers. The band gap of the laminated superlattice layers is almost the same as ZnO. ZnTe shows p type conductivity with doping N as an impurity. The impurity diffusion of N from the ZnTe layer of N dope and movement of a hole are produced over ten molecular layer among ZnO layers.

[0120] Thus, grown-up ZnO/ZnTe superlattice layers show the character as a p type conductive layer as a whole.

[0121] The thickness of ZnTe was limited to one molecular

layer. It is the thickness below critical thickness and distortion generated in a growth phase can be suppressed small. Surface morphology of a growth phase can be made good.

[0122] If the flow of N to ZnTe is set to 0.05 or less ccm on the above-mentioned growing condition, the doping quantity of N to the inside of ZnTe will be stopped below at $1\times10^{20}cm^{-3}$.

[0123] Preferably, N concentration doped by ZnO by diffusion etc. is stopped lower than the doping concentration of N doped by ZnTe.

[0124] The diode which has p-n junction can be created using the production technology of the above-mentioned p type ZnO system single crystal layer, and the formation art of an ohmic electrode over a p type system ZnO single crystal.

[0125] In order to form the diode which has p-n junction using a ZnO system single crystal, While from the above-mentioned process 1 to the process 6, the process of forming a n type ZnO single crystal layer between the process of growing up the high-temperature-growth non-doped ZnO single crystal layer of the process 4, and the process of forming the p type ZnO single crystal layer of 5 is performed. A n type ZnO single crystal may be grown up instead of a high-temperature-growth non-doped ZnO single crystal layer. Ga used as a dopant of a n type impurity during growth of a ZnO single crystal using the Ga port 21 is doped.

[0126] The formed n type ZnO single crystal layer is 1

micrometer in thickness. The doped quantity of Ga is 1x10 $^{18}cm^{-3}$.

[0127] On a n type ZnO single crystal layer, a p type ZnO single crystal layer is formed.

[0128] After the end of crystal growth, by the liquid phase etching method or a gas-phase-etching method, a p type ZnO single crystal layer is etched, and the surface of a n type ZnO single crystal layer is exposed.

[0129] On the surface of the exposed n type ZnO single crystal layer, materials, such as aluminum, are used, for example and the 1st electrode is formed.

[0130] By the above-mentioned process of 6, and the same process, the 2nd electrode is formed using materials, such as nickel/Au, for example after that.

[0131] Of the above-mentioned process, the p-n junction diode using a ZnO single crystal is formed.

[0132] In the above-mentioned structure, if the voltage of plus is impressed to the 2nd electrode to the 1st electrode, forward current will flow into p-n junction. The minority carrier (electron) poured in into the p type ZnO single crystal layer and the majority carrier (electron hole) in a p type ZnO single crystal layer carry out radiation recombination. The light which has energy almost equal to the energy gap of a forbidden band in the case of the recombination of an electron and an electron hole occurs. That is, electric energy is transformed into luminous energy.

[0133] An OPTO semiconductor device is made using the above-mentioned p-n junction diode structure.

[0134]The semiconductor device (OPTO semiconductor device) by a 2nd embodiment of this invention is explained.

[0135]The section structure of LED (LightEmittingDiode) which used the p-n junction of a p type ZnO single crystal layer and a n type ZnO single crystal layer is shown in drawing 5.

[0136]The non-doped low-temperature growth ZnO buffer layer 305 with a thickness of 10 nm by which low-temperature growth of the LED shown in drawing 5 was carried out on it with the sapphire substrate 301, The 1-micrometer-thick high-temperature-growth non-doped ZnO single crystal layer 307 grown-up on it, The p type above-mentioned ZnO system single crystal layer 315 which carried out the ** dope of the 1-micrometer-thick n type (Ga dope: $1\times10^{18}cm^{-3}$) high-temperature-growth ZnO single crystal layer 311 grown-up on it, and 100-nm-thick N and Ga which were formed on it is included.

[0137]It is in contact with the n type ZnO single crystal layer 311 with the 1st electrode 321 that consists of aluminum.

[0138]In order to form a n type ZnO layer, other three group elements, such as aluminum, may be doped instead of Ga.

[0139]The p type ZnO system single crystal layer 315 formed by the ** dope (N, Ga) is processed into island shape.

[0140]The p type ZnO single crystal layer 315 processed into island shape is covered with the insulator layer 318 which consists of Si_3N_4, for example. The opening of an

approximate circle form penetrates the insulator layer 318 in the upper surface of the p type ZnO single crystal layer 315, and is formed in it, for example.

[0141] On the upper surface periphery of the p type ZnO single crystal layer 315, the 2nd electrode 325 (the 1st metal layer 325a (nickel) and the 2nd metal layer 325b (Au)) of ring shape is formed. In at least a part of the undersurface, the 2nd electrode of ring shape contacts the periphery of the upper surface of p type ZnO layer 315. The portion of the method of the outside of a diameter direction of the 2nd electrode 235 of ring shape has structure which ran aground on the insulator layer 318.

[0142] In the above-mentioned structure, if the voltage of plus is impressed to the 2nd electrode 325 (325a, 325b) to the 1st electrode 321, forward current will flow into p-n junction. The minority carrier (electron) poured in into the p type ZnO single crystal layer 315 and the majority carrier (electron hole) in the p type ZnO single crystal layer 315 carry out luminescent recombination. The light which has energy equal to the energy gap of the forbidden band of ZnO in the case of the recombination of an electron and an electron hole is emitted from the opening 327. The wavelength of emitted light is about 370 nm.

[0143] Drawing 6 is a sectional view showing the 1st modification of the semiconductor device by a 2nd embodiment of this invention.

[0144] Drawing 6 (a) is a sectional view showing the structure of LED (LightEmittingDiode) containing the p-n

junction diode using ZnO of Ga dope as an n-type semiconductor using the superlattice which consists of ZnTe of a ZnO/N dope as a p-type semiconductor.

[0145] Drawing 6 (b) is a sectional view showing the superstructure which consists of ZnO/ZnTe.

[0146] LED is provided with the following as shown in drawing 6 (a).

Sapphire substrate 301.

The non-doped ZnO buffer layer 305 with a thickness of 10 nm by which low-temperature growth was carried out on it.

The 1-micrometer-thick high-temperature-growth non-doped ZnO single crystal layer 307 grown-up on it.

Superlattice layers 316 (about 100 nm as total thickness) by which ZnO of 30 layers which grew on it and was formed on it with 1-micrometer-thick n type (Ga dope: $1 \times 10^{18} cm^{-3}$) ZnO layer 311, and ZnTe (N) were laminated by turns.

[0147] As shown in drawing 6 (b), superlattice layers are used as a p type ZnO system single crystal layer instead of the ** doped p type ZnO single crystal 315 (drawing 5). The superlattice layers 316 of a undoped ZnO layer and the ZnTe layer of N dope are used on n type ZnO layer 311.

[0148] the superlattice layers 316 -- ZnO layers 331a and 331b and ... it is formed by the crosswise lamination of 331z and the ZnTe layers 333a, 333b, ..., 333z. ZnO layers 331a and 331b and ... each of 331Z is ten molecular layers, for example -- the ZnTe layers 333a and 333b and ... each of 333z is one molecular layer, for example.

[0149] The total thickness of the superlattice layers 316

is about 100 nm, for example. ZnTe is laminated for ZnO at a rate of one molecular layer to ten molecular layers. The band gap of the laminated superlattice layers is almost the same as ZnO. ZnTe shows p type conductivity with doping N as an impurity. The impurity diffusion of N and movement of a hole arise from the ZnTe layer of N dope over ZnO layer 10 molecular layer to a ZnO layer.

[0150] On the ZnO/ZnTe superlattice layers which show p type conductivity, by the same method as the ohmic electrode for p type ZnO single crystals by a 1st embodiment of the above. For example, ohmic junction can be acquired to p type ZnO/ZnTe superlattice layers by forming the electrode which consists of nickel/Au.

[0151] It is in contact with n type ZnO layer 311 (drawing 6 (a)) with the 1st electrode 321 (aluminum).

[0152] In order to form a n type ZnO layer, other three group elements, such as aluminum, may be doped instead of Ga.

[0153] The superlattice layers 316 are processed into island shape. The lateral part is covered with the insulator layer 318 in which the superlattice layers 316 processed into island shape consist of SiN(s), for example. The opening of an approximate circle form is formed in the upper surface of the superlattice layers 316 among the insulator layers 318, for example. Coating protection of the side is carried out with the insulator layer 318 at least among the superlattice layers 316 processed into island shape.

[0154] For example, it has an opening, the 2nd electrode

325 (325a, 325b) of ring shape is formed in the periphery of the superlattice layers 316. As for the 2nd electrode of ring shape, the undersurface by the side of the inner circumference contacts the periphery of the upper surface of the superlattice layers 316. The peripheral part has structure which ran aground on the insulator layer 318 among the 2nd electrode.

[0155]In the above-mentioned structure, if the voltage of plus is impressed to the 2nd electrode 325 to the 1st electrode 321, forward current will flow into p-n junction. The minority carrier (electron) poured in into the p type superlattice layers 316 and the majority carrier (electron hole) in the p type superlattice layers 316 carry out radiation recombination. The light which has energy almost equal to the energy gap of a forbidden band in the case of the recombination of an electron and an electron hole emits from said opening. That is, electric energy is transformed into luminous energy.

[0156]The 2nd modification of the semiconductor device (LED) by a 2nd embodiment is shown in drawing 7.

[0157]The non-doped low-temperature growth ZnO buffer layer 405 with a thickness of 10 nm by which low-temperature growth of the LED shown in drawing 7 was carried out on it with the sapphire substrate 401, The 1-micrometer-thick high-temperature-growth non-doped ZnO single crystal layer 407 grown-up on it, The p type ZnO system single crystal layer 415 which carried out the ** dope of the 1-micrometer-thick n type (Ga dope: $1\times10^{18}cm^{-3}$) high-temperature-growth ZnO single crystal layer

411 grown-up on it, and 100-nm-thick N and Ga which were formed on it is included.

[0158]It is in contact with the n type ZnO single crystal layer 411 with the 1st electrode 421 that consists of aluminum.

[0159]In order to form a n type ZnO layer, other three group elements, such as aluminum, may be doped instead of Ga.

[0160]The p type ZnO system single crystal layer 415 formed by the ** dope (N, Ga) is processed into island shape.

[0161]The p type ZnO system single crystal layer 415 processed into island shape is covered with the insulator layer 418 which consists of Si_3N_4, for example. The opening of an approximate circle form penetrates the insulator layer 418 in the upper surface of the p type ZnO single crystal layer 415, and is formed in it, for example.

[0162]On the surface of the p type ZnO system single crystal layer 415, the 2nd electrode 425 (the 1st metal layer 425a, for example, nickel, and the 2nd metal layer 425b, for example, Au) is formed. In at least a part of the undersurface, the 2nd electrode 425 contacts the surface of the p type ZnO system single crystal layer 415. The portion of the method of the outside of a diameter direction of the 2nd electrode 425 (425a, 425b) formed in ring shape has structure which ran aground on the insulator layer 418. The 2nd electrode 425 (425a, 425b) has the electrode structure of nickel/Au, for example.

[0163]On the 2nd electrode 425 (425a, 425b), the reflector

427 is formed so that the opening currently formed in the 2nd electrode 425 (425a, 425b) of the above may also be covered. The reflector 427 is formed, for example with the metallic material with high reflectance like aluminum or Ag.

[0164] In the above-mentioned structure, if the voltage of plus is impressed to the 2nd electrode 425 (425a, 425b) to the 1st electrode 421, forward current will flow into p-n junction. The minority carrier (electron) poured in into the p type ZnO system single crystal layer 415 and the majority carrier (electron hole) in the p type ZnO system single crystal layer 415 carry out luminescent recombination. The light which has energy almost equal to the energy gap of a forbidden band in the case of the recombination of an electron and an electron hole occurs. That is, electric energy is transformed into luminous energy.

[0165] The generated light penetrates the sapphire substrate 401. It is reflected by the reflector 427 and the sapphire substrate 401 and the light emitted to a reverse side penetrate the sapphire substrate 401 eventually. The wavelength of the light which penetrates the sapphire substrate 401 is about 370 nm.

[0166] The 3rd modification of the semiconductor device (LED) by a 2nd embodiment of the above is shown in drawing 8.

[0167] LED shown in drawing 8 is LED of a flip chip type.

[0168] LED of this flip chip type has the structure of LED shown in drawing 5, and the same structure.

[0169]The non-doped low-temperature growth ZnO buffer layer 305 with a thickness of 10 nm by which low-temperature growth was carried out more on it with the sapphire substrate 301 at details, The 1-micrometer-thick high-temperature-growth non-doped ZnO single crystal layer 307 grown-up on it, The above-mentioned p type ZnO system single crystal layer 315 which carried out the ** dope of the 1-micrometer-thick n type (Ga dope: $1x10^{18}cm^{-3}$) high-temperature-growth ZnO single crystal layer 311 grown-up on it, and 100-nm-thick N and Ga which were formed on it is included.

[0170]It is in contact with the n type ZnO single crystal layer 311 with the 1st electrode 321 that consists of aluminum.

[0171]The p type ZnO system single crystal layer 315 formed by the ** dope (N, Ga) is processed into island shape.

[0172]On the partial area of the p type ZnO system single crystal layer 315, the 2nd electrode 325 (325a, 325b) is formed. The 2nd electrode 325 (325a, 325b) has the electrode structure of nickel/Au, for example. The reflector 331 which consists of a metallic material with high reflectance, such as aluminum and Ag, for example is formed in the rear face of the sapphire substrate 301.

[0173]The rear face (side in which the reflector 331 is formed) of the sapphire substrate 301 of LED which has the above-mentioned structure is turned up, and it carries on the glass substrate 341 currently prepared separately.

[0174]The 1st and 2nd circuit patterns 345a and 345b

formed in the predetermined field on the glass substrate 341, for example of Ti/Au are formed more in details.

[0175]The 1st circuit pattern 345a is electrically connected with the 1st electrode 311 via the vamp 347.

[0176]The 2nd circuit pattern 345b is directly electrically connected with the 2nd electrode 325 (325a, 325b).

[0177]In the above-mentioned structure, if voltage is impressed between the 1st and 2nd circuit patterns 345a and 345b so that the voltage of plus may be impressed to the 2nd electrode 325 (325a, 325b) to the 1st electrode 321, forward current will flow into p-n junction. The minority carrier (electron) poured in into the p type ZnO system single crystal layer 315 and the majority carrier (electron hole) in the p type ZnO system single crystal layer 315 carry out luminescent recombination. In the case of the recombination of an electron and an electron hole, the light which has energy equal to the energy gap of the forbidden band of ZnO is emitted, and the glass substrate 341 is penetrated. It is reflected by the reflector 331 and the glass substrate 341 and the light emitted to a reverse side penetrate the glass substrate 341 eventually. The wavelength of the light which penetrates the glass substrate 341 is about 370 nm.

[0178]In this above-mentioned embodiment, although LED was explained as an example of the semiconductor device using the p-n junction of a p type ZnO system single crystal layer and a n type ZnO single crystal layer, it is also possible to form a laser element combining a p type

ZnO system single crystal layer and a n type ZnO single crystal layer. In addition, it cannot be overemphasized that it is also possible to manufacture the semiconductor device which combined electron devices, such as FET and a bipolar transistor, other optical devices, and these combining a p type ZnO single crystal layer.

[0179] As mentioned above, although this invention was explained along with the embodiment, this invention is not restricted to these. Various conditions and other process parameters of crystal growth can also be chosen. In addition, it is obvious ****** in a person skilled in the art for various change, improvement, combination, etc. to be possible.

[0180]

[Effect of the Invention] The semiconductor device which has a good ohmic electrode to a p type ZnO system single crystal layer can be formed.

[0181] When a semiconductor device is formed, operating voltage can be dropped and low power consumption becomes possible. Since the parasitic resistance resulting from an ohmic electrode can be reduced, the influence of generation of heat in a semiconductor device can be suppressed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a sectional view showing the outline of the MBE device for growing up the crystal structure

included in the semiconductor device by a 1st embodiment of this invention.

【Drawing 2】It is a sectional view showing the structure of the semiconductor device by a 1st embodiment of this invention.

【Drawing 3】It is a figure showing the current/voltage characteristics of the semiconductor device by a 1st embodiment of this invention.

【Drawing 4】It is a timing chart which shows the sequence method of the shutter for growing up the crystal structure included in the semiconductor device by the 1st modification of a 1st embodiment of this invention.

【Drawing 5】It is a semiconductor device by a 2nd embodiment of this invention, and is a sectional view showing the structure which applied the semiconductor device by a 1st embodiment of the above to LED.

【Drawing 6】It is a sectional view of the crystal structure by the 1st modification of the semiconductor device by a 2nd embodiment of this invention. Drawing 6 (a) is a sectional view showing the whole structure. Drawing 6 (b) is a sectional view showing the structure of superlattice layers.

【Drawing 7】It is a sectional view showing the structure which applied the semiconductor device by the 2nd modification of a 2nd embodiment of this invention to LED.

【Drawing 8】It is a sectional view showing the structure which applied the semiconductor device by the 3rd modification of a 2nd embodiment of this invention to LED.

【Description of Notations】

A RS-MBE device

C Control device

P Vacuum pump

S Substrate

1 Chamber

3 Substrate holder

3a Heater

5 Thermo couple

7 Manipulator

11 The port for Zn

15 Zn raw material

17 Knudsen cell

21 O radical port

31 N radical port

100 ZnO board

101 ZnO buffer layer (low-temperature growth ZnO buffer layer)

103 ZnO single crystal layer (high-temperature-growth ZnO single crystal layer)

105 N type ZnO system single crystal layer

107 P type ZnO system single crystal layer

108 Electrode

108a The 1st metal layer

108b The 2nd metal layer

301 Sapphire substrate

305 ZnO buffer layer (low-temperature growth ZnO buffer layer)

307 Undoped ZnO single crystal layer (high-temperature-growth ZnO single crystal layer)

311 N type ZnO single crystal layer (high-temperature-growth ZnO single crystal layer)

315 P type ZnO system single crystal layer (high-temperature-growth ZnO single crystal layer)

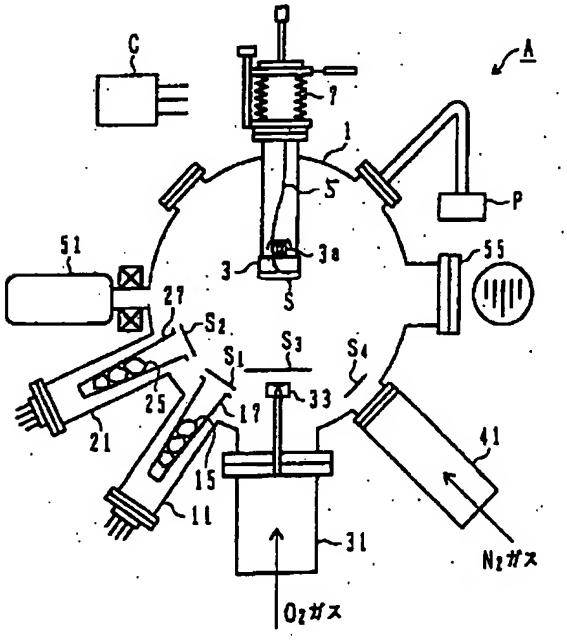
318 Insulator layer

321 The 1st electrode

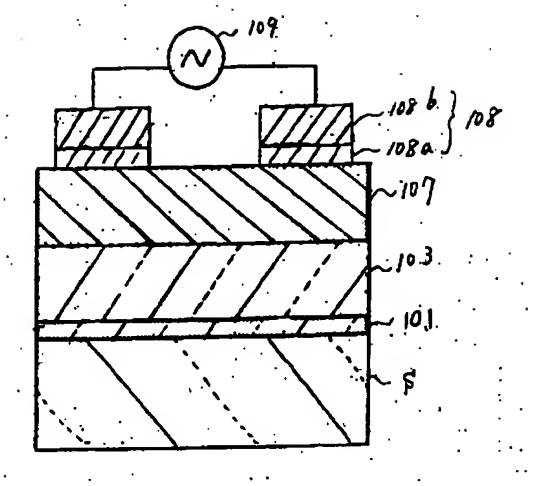
325 The 2nd electrode

DRAWINGS

【Drawing 1】



【Drawing 2】



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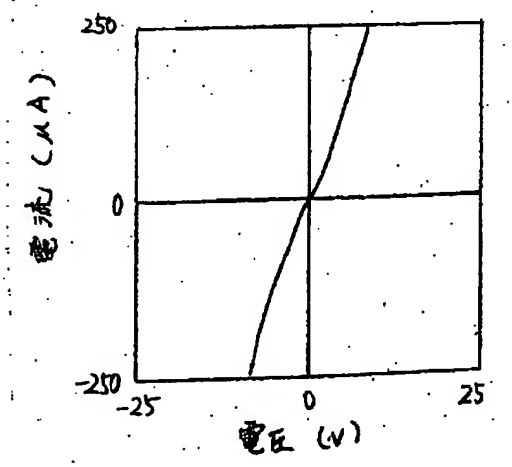
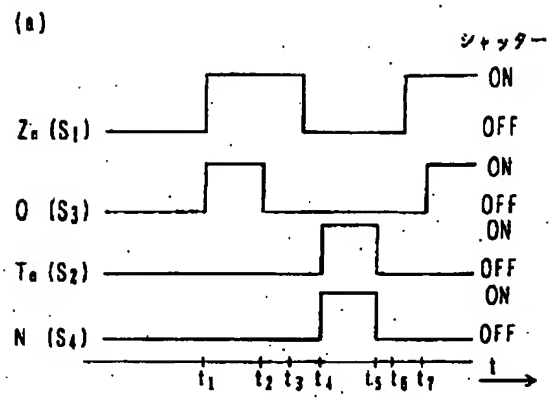
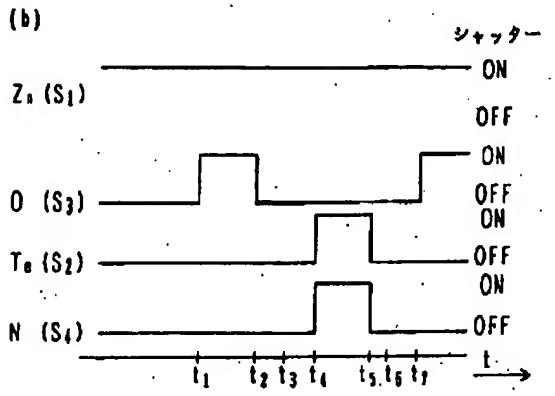
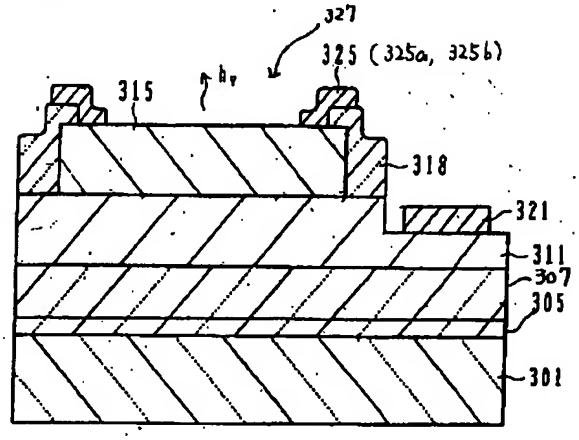


【Drawing 4】

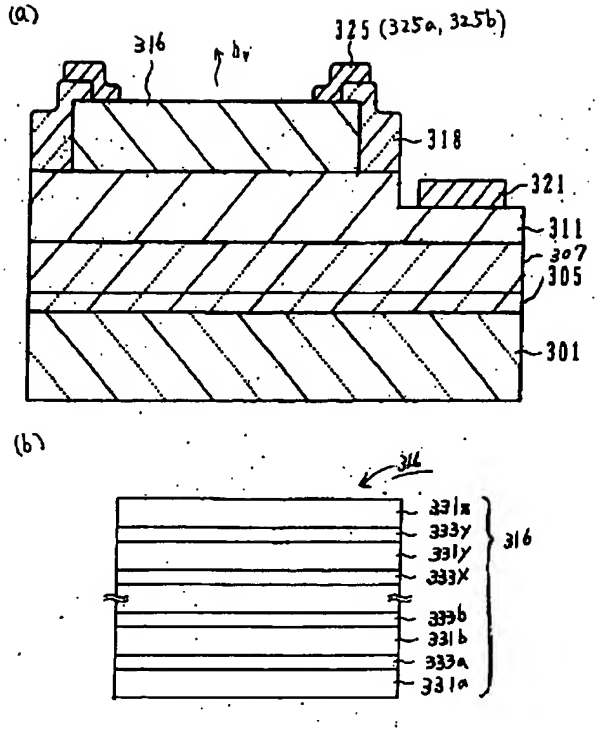




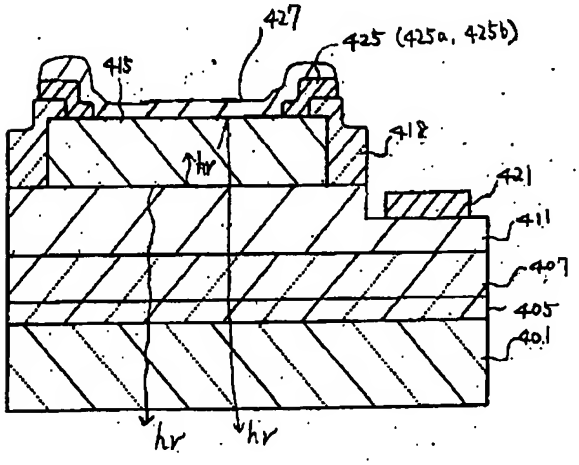
【Drawing 5】



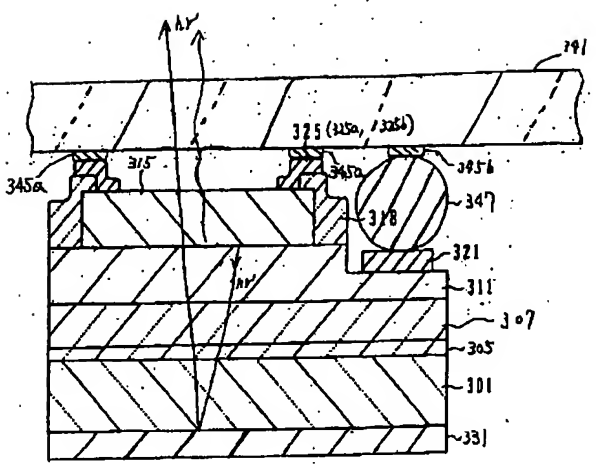
【Drawing 6】



[Drawing 7]



[Drawing 8]



WRITTEN AMENDMENT

【Written amendment】

【Filing date】January 19, Heisei 12 (2000.1.19)

【Amendment 1】

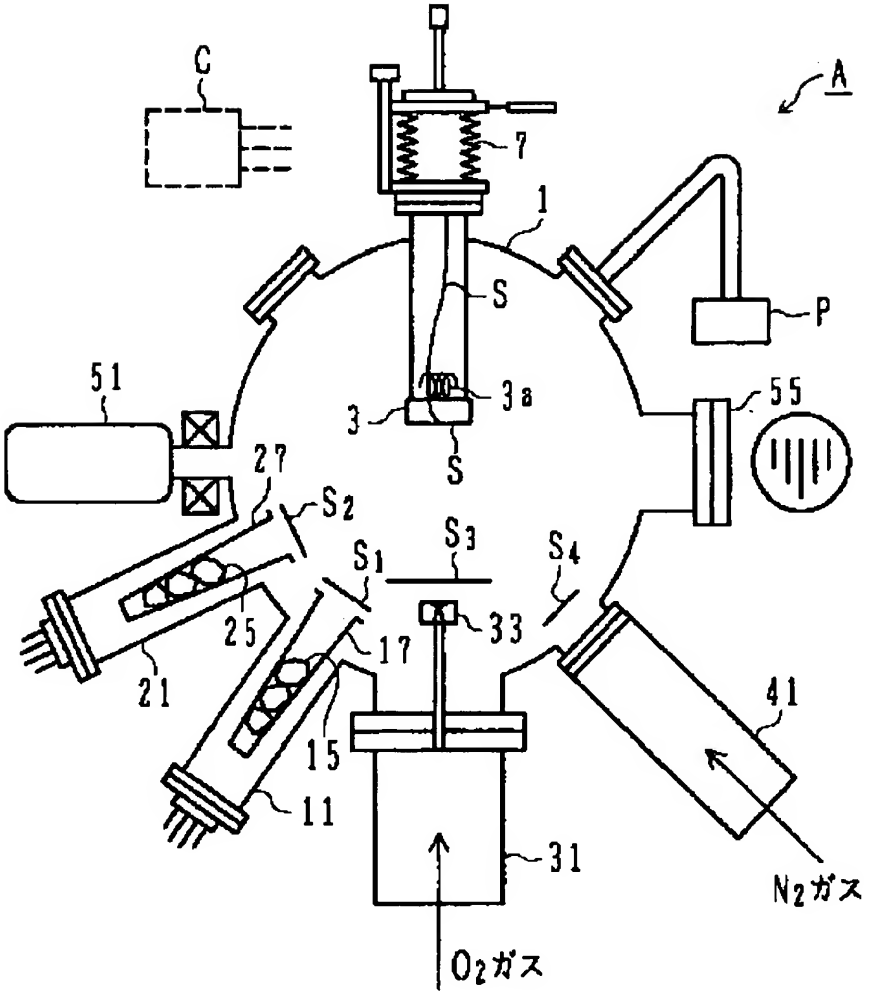
【Document to be Amended】DRAWINGS

【Item(s) to be Amended】Complete diagram

【Method of Amendment】Change

【Proposed Amendment】

【Drawing 1】



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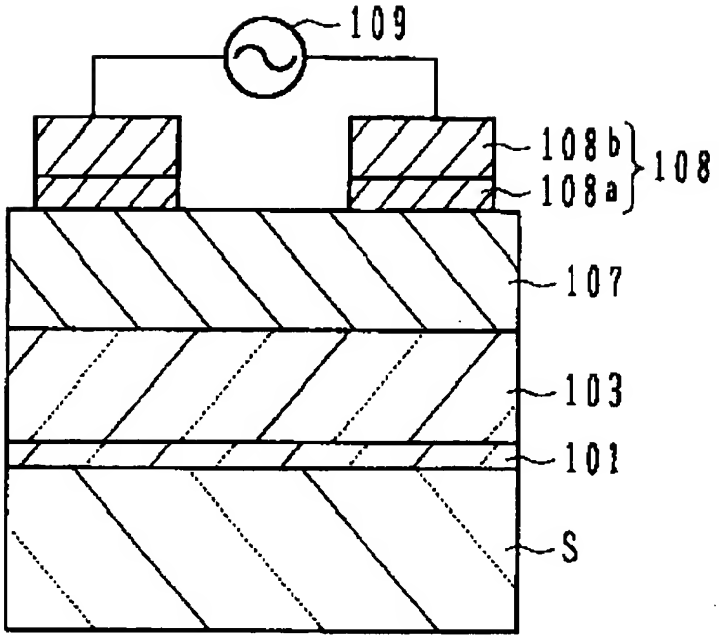

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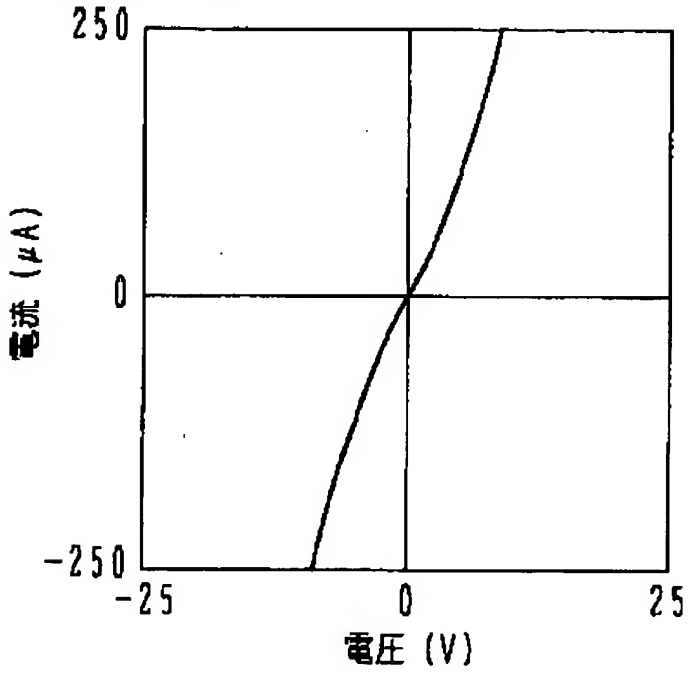
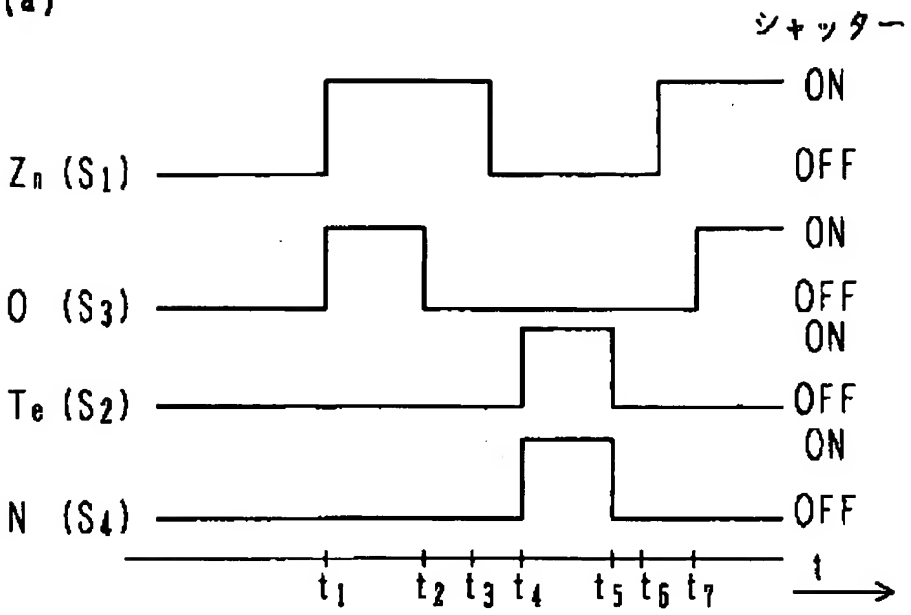
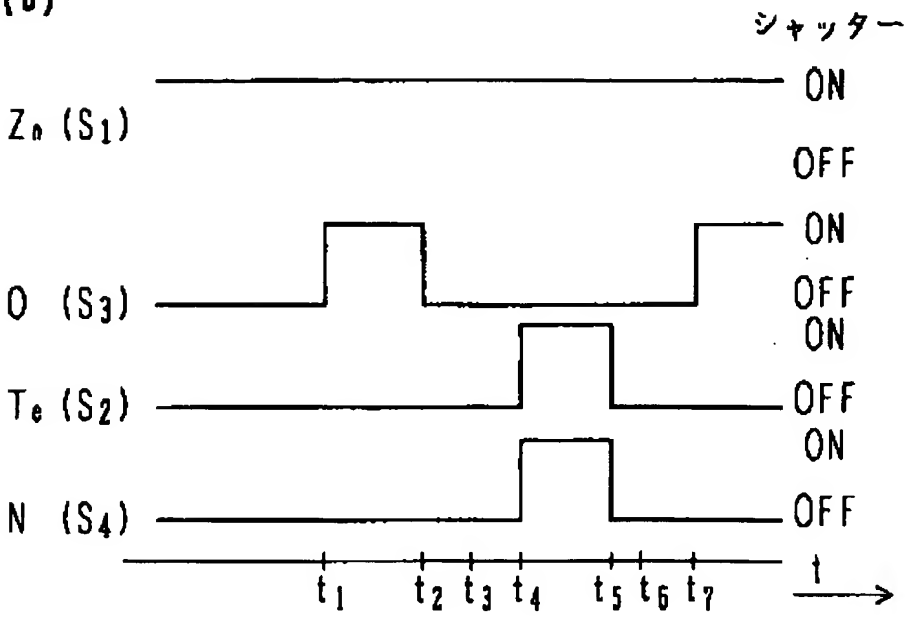


【Drawing 4】

(a)


シャッター
ON
OFF
Zn (S1)
ON
OFF
O (S3)
ON
OFF
Te (S2)
ON
OFF
N (S4)
t1 t2 t3 t4 t5 t6 t7
t

(b)


シャッター
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Zn (S1)
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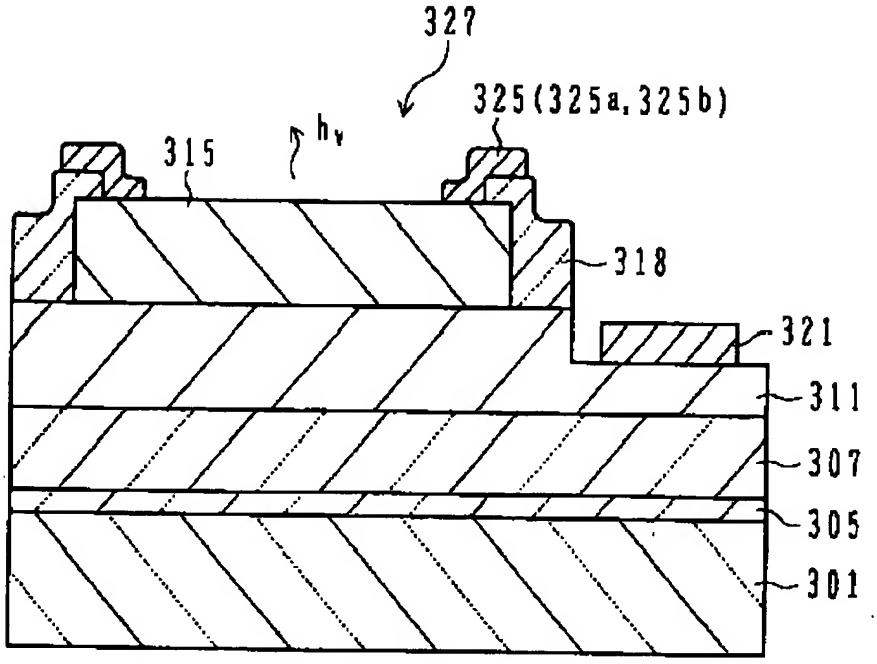
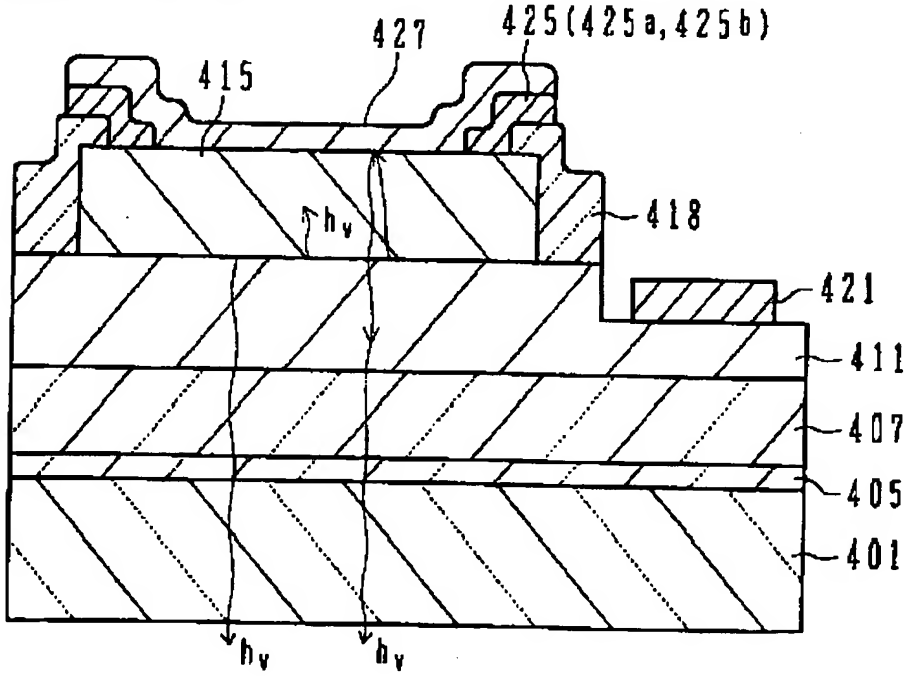
t1 t2 t3 t4 t5 t6 t7
t

[Drawing 5]

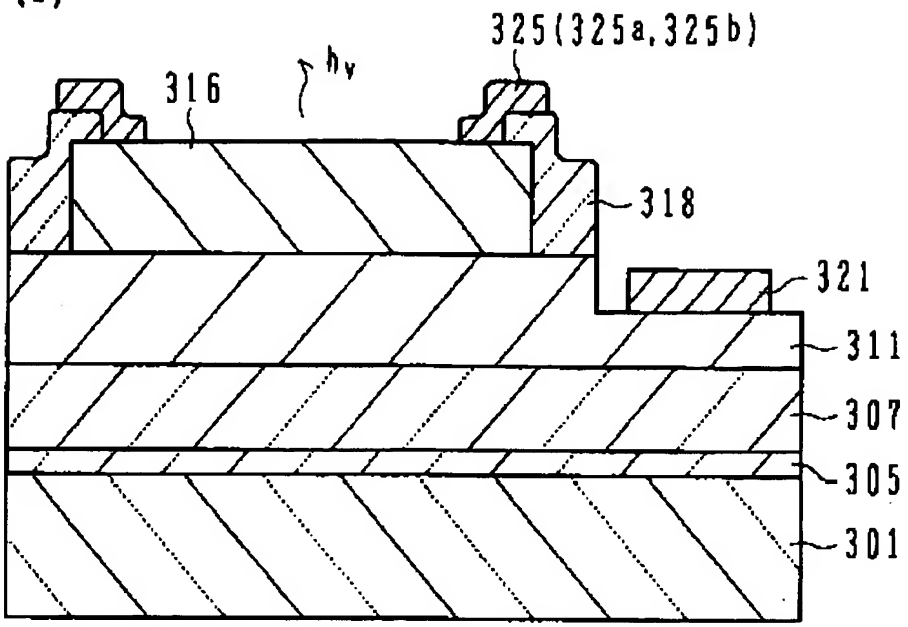


【Drawing 7】

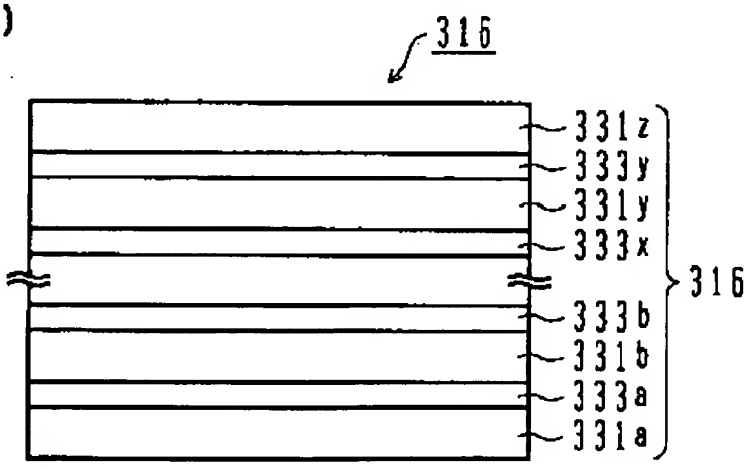


【Drawing 6】

(a)


325(325a,325b)
hν
316
318
321
311
307
305
301

(b)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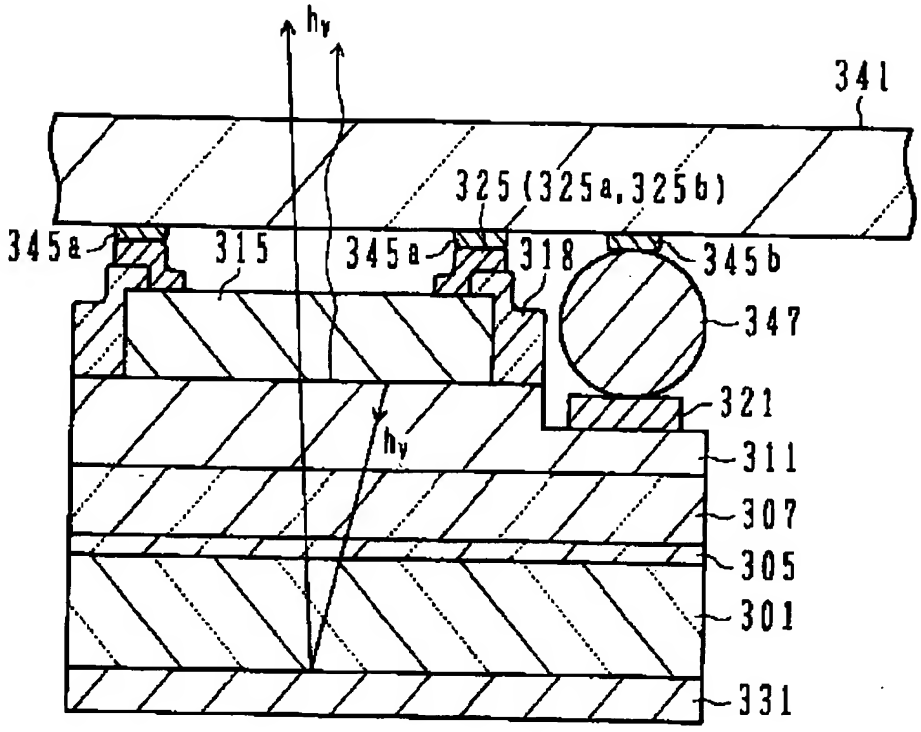
331y
333x
316
333b
331b
333a
331a

[Drawing 8]



[Translation done.]